AAT2402M/2402S

Sixteen-Channel White LED Driver Solution with Full LED Current and Timing Control

General Description

The AAT2402M/2402S is a highly integrated, high efficiency white LED backlight solution for large size LCD panels used in LCD TVs. To accommodate power requirements, the solution consists of two devices, a master device (AAT2402M) and a slave device (AAT2402S). The devices operate from a regulated 24V DC power supply. The master device supplies a 40V rail to drive 10 series LEDs with a typical V_F of 3.6V. 16 precision current sinks split evenly between the master and slave devices provide constant current drive for up to 160 white LEDs.

A SPI compatible interface operates up to 30MHz, allowing fast, independent digital control of each current sink. Full scale LED current is programmed from 30mA to 100mA using an external resistor. LED brightness variation is compensated by setting relative current sink magnitudes with an 8-Bit Dot Correction register for each LED current sink.

The AAT2402M/2402S provides a 12-bit programmable phase delay per LED current sink that can be used to synchronize the LEDs to V_{SYNC}. Device addressing provides for up to 256 LED strings. A 12-bit programmable Gray Scale PWM brightness setting is generated via a clock from a PLL synchronized to V_{SYNC}, or from the external GSCLK pin.

The AAT2402M/2402S provides fault handling and fault reporting through the interface. If LEDs are shorted on one or more strings, the current sinks will maintain operation due to the high voltage rating of the outputs. However, a fault condition will be reported on the open drain FAULT pin. Similarly, if an open circuit is detected or an over-temperature condition arises, the fault is reported on the FAULT pin. When a fault is reported, the nature of the fault condition can be read through the serial interface.

The AAT2402M boost converter provides an output voltage regulated by the string with the highest voltage requirement allowing a wide range of LED characteristics, while maintaining the lowest possible power dissipation. The boost switching frequency is 600kHz to allow for optimum efficiency with the smallest external filter. Alternatively, the device may be synchronized to an external clock. Current mode control provides fast response to line and load transients. Thermal protection circuitry shuts down the boost converter and the current sinks in the event of an over-temperature condition.

The AAT2402M and AAT2402S are available in Pb-free, thermally enhanced 36-pin 5x5mm TQFN packages.

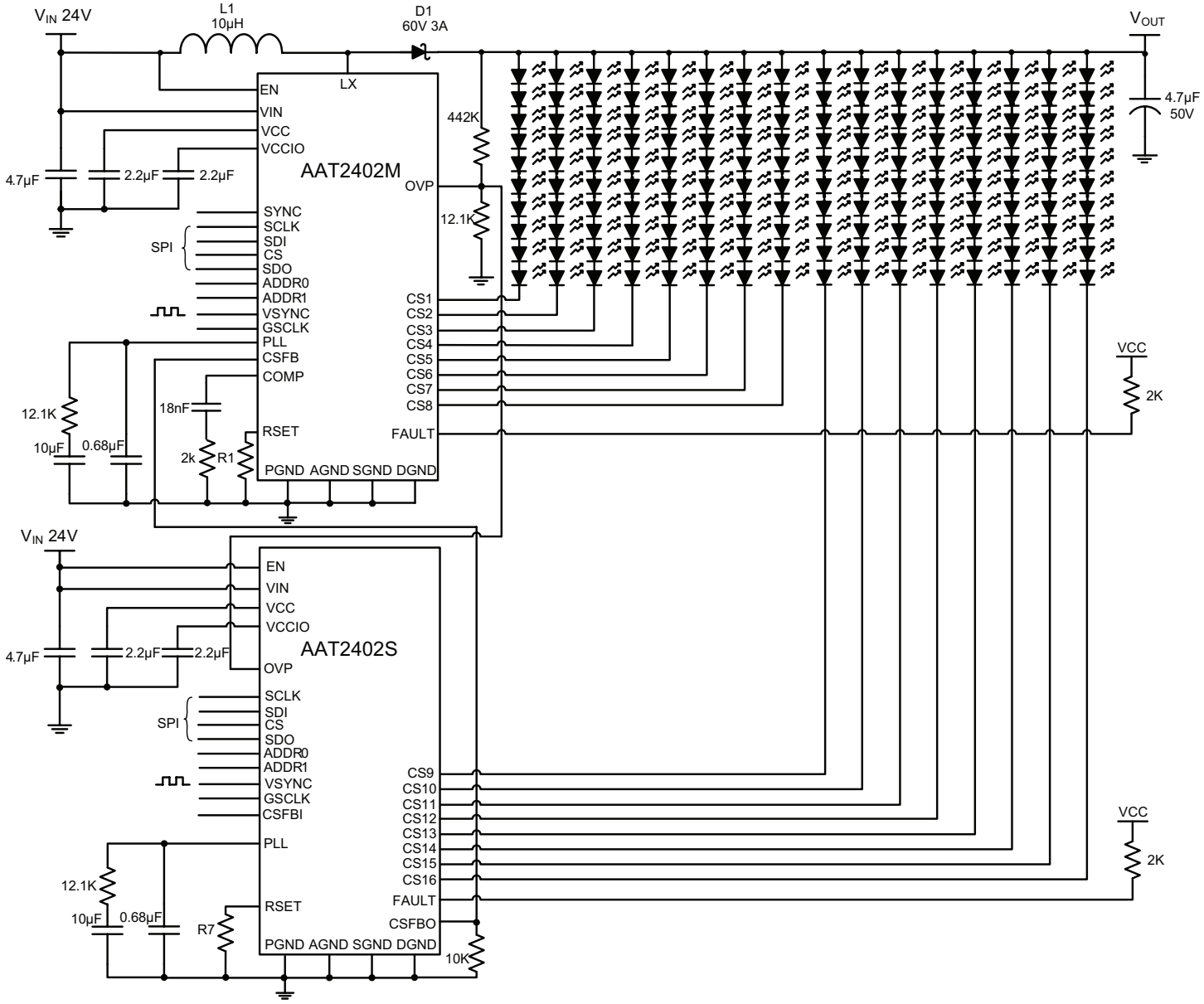
Features

- Secondary Latch Function
  - Dot Correction to VSYNC Signal
  - Gray Scale to PWM Signal
- V_{IN} Range: 10.8V – 28V
- Integrated Boost Converter
  - $V_{OUT(MAX)}$: 40V
  - $I_{OUT(MAX)}$: 1.6A
- Up to 95% Efficiency
- Switching Frequency Options
  - 600 kHz
  - Sync to External Clock (optional)
- 16 LED Current Sinks up to 100mA/ch
  - ±2.5% Accuracy (60mA)
  - ±2.0% Matching (60mA)
- SPI Interface
  - Digitally Programmable Individual Channels
  - Up to 30MHz Clock Speed
  - Read/Write Registers
- Precision PWM Digital Brightness Control
  - 12-bit Individual Gray Scale PWM Brightness
  - 12-bit Individual Channel Phase Delay
  - 8-bit Individual Current Setting (Dot Correction)
  - V_{SYNC} Derived Internal Oscillator
- V_{SYNC} PWM and Delay Synchronization
- Device Addressing
  - 16 Possible Address Settings
  - Up to 256 Current Sinks
- Fault Reporting
- Integrated Fault Protection
  - Open/Short LED(s)
  - Current Limit Protection
  - Over-Voltage Protection
  - Over-Temperature Protection
- Soft-Start to Minimize Inrush Current
- TQFN55-36 Low Profile Package
- -40°C to +85°C Temperature Range

Applications

- Large Size LCD TV, Panels
- White LED Backlight

Typical Application Circuit



AAT2402M Pin Descriptions

Pin #	Symbol	Function	Description
1	CS5	O	Output current sink 5[1].
2	CS6	O	Output current sink 6[1].
3	CS7	O	Output current sink 7[1].
4	CS8	O	Output current sink 8[1].
5	SGND	GND	Current sink ground. Connect to GND as closely as possible to the device.
6	CS4	O	Output current sink 4[1].
7	CS3	O	Output current sink 3[1].
8	CS2	O	Output current sink 2[1].
9	CS1	O	Output current sink 1[1].
10	RSET	I	Resistor for setting maximum current sink DC level. Connect a resistor between this pin and the AGND pin.
11	EN	I	Logic high enable pin. Apply a logic high voltage after power is applied to VIN or connect to VIN through a RC time delay network to enable the device.
12	FAULT	O	Open drain fault signal. Pull up to logic supply with external resistor.
13	PLL	I/O	PLL compensation. Connect associated network between this pin and AGND.
14, 32	AGND	GND	Analog ground. Connect to GND with one single connection.
15	DGND	GND	Digital ground. Connect to GND as closely as possible to the device.
16	VIN	I	IC and boost converter power supply.
17	VCC	I/O	Internally regulated power supply. Decouple with 2.2µF/6.3V capacitor to AGND.
18	VCCIO	I/O	Internally regulated power supply (3.3V) for SDO. Decouple with 2.2µF/6.3V capacitor to DGND.
19	SDO	O	SPI interface serial data output.
20	COMP	I	Boost converter compensation. Connect external resistor and capacitor to this pin and AGND.
21	CSFB	I	Current sink feedback. Connect to slave device CSFBO with a 10kΩ pull-down resistor.
22	SYNC	I	Connect to an external clock for synchronization Connect to PGND if not used.
23	N/C		No connect
24, 25	LX	O	Switching node of boost converter. Connect a 10µH inductor between this pin and VIN. Connect a Schottky diode between this pin and the boost output capacitor.
26, 27	PGND	GND	Power ground of boost converter integrated NMOS switching device. Boost output capacitor must be placed very close to this pin.
28	ADDR1	I	MSB device address. Connect to VCC, GND, SDI or leave unconnected to set address.
29	ADDR0	I	LSB device address. Connect to VCC, GND, SDI or leave unconnected to set address.
30	VSYNC	I	Vertical sync. PWM operation synchronization and reset.
31	GSCLK	I	PWM clock. Apply clock or connect to GND if not used.
33	SCLK	I	SPI interface serial clock.
34	SDI	I	SPI interface serial data input.
35	CSB	I	SPI interface active low chip select.
36	OVP	I	Over-voltage protection pin. Connect resistive divider between VOUT and GND.
EP			Exposed paddle. Connect to PCB GND plane. PCB paddle heat sinking should maintain acceptable junction temperature.

1. Unused current sink channels must be terminated. Refer to the Channel Disable paragraph in the Application Information section of this datasheet.

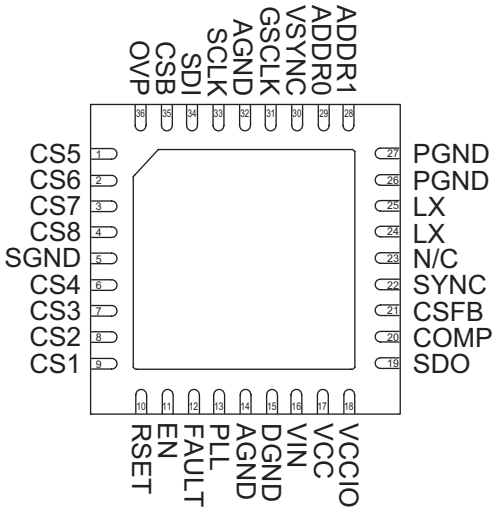
AAT2402S Pin Descriptions

Pin #	Symbol	Function	Description
1	CS5	O	Output current sink 5[1].
2	CS6	O	Output current sink 6[1].
3	CS7	O	Output current sink 7[1].
4	CS8	O	Output current sink 8[1].
5	SGND	GND	Current sink ground. Connect to GND as closely as possible to the device.
6	CS4	O	Output current sink 4[1].
7	CS3	O	Output current sink 3[1].
8	CS2	O	Output current sink 2[1].
9	CS1	O	Output current sink 1[1].
10	RSET	I	Resistor for setting maximum current sink DC level. Connect a resistor between this pin and the AGND pin.
11	EN	I	Logic high enable pin. Apply a logic high voltage after power is applied to the VIN, or connect to VIN through a RC time delay network to enable the device.
12	FAULT	O	Open drain fault signal. Pull up to logic supply with external resistor.
13	PLL	I/O	PLL compensation. Connect associated network between this pin and AGND.
14, 32	AGND	GND	Analog ground. Connect to GND with one single connection.
15	DGND	GND	Digital ground. Connect to GND as closely as possible to the device.
16	VIN	I	IC and boost converter power supply.
17	VCC	I/O	Internally regulated power supply. Decouple with 2.2µF/6.3V capacitor to AGND.
18	VCCIO	I/O	Internally regulated power supply (3.3V) for SDO. Decouple with 2.2µF/6.3V capacitor to DGND.
19	SDO	O	SPI interface serial data output.
20, 22, 24, 25, 26, 27	AGND	GND	Connect to GND with one single connection.
21	CSFBO	O	Current sink feedback output. Connect to master device CSFB with a 10kΩ pull-down resistor
23	CSFBI	I	Current sense feedback input. Connect to VCC if not used.
28	ADDR1	I	MSB device address. Connect to VCC, GND, SDI or leave unconnected to set address.
29	ADDR0	I	LSB device address. Connect to VCC, GND, SDI or leave unconnected to set address.
30	VSYNC	I	Vertical sync. PWM operation synchronization and reset.
31	GSCLK	I	PWM clock. Apply clock or connect to GND if not used.
33	SCLK	I	SPI interface serial clock.
34	SDI	I	SPI interface serial data input.
35	CSB	I	SPI interface active low chip select.
36	OVP	I	Over-voltage protection pin. Connect resistive divider between VOUT and GND.
EP			Exposed paddle. Connect to PCB GND plane. PCB paddle heat sinking should maintain acceptable junction temperature.

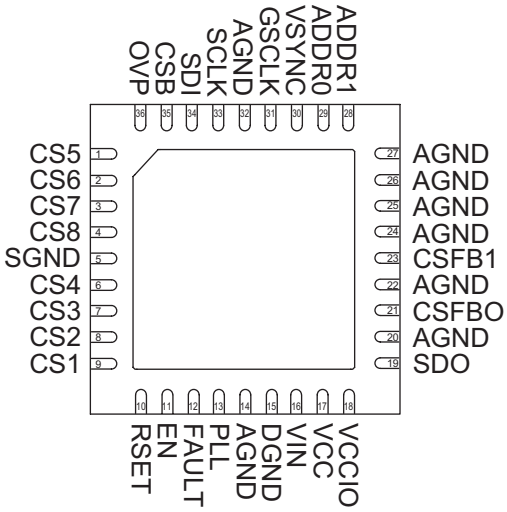
1. Unused current sink channels must be terminated. Refer to the Channel Disable paragraph in the Application Information section of this datasheet.

Pin Configuration

AAT2402M
TQFN55-36
(Top View)



AAT2402S
TQFN55-36
(Top View)



Absolute Maximum Ratings[1]

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
V_{LX}	LX Voltage to GND	45	V
$V_{IN,EN}$	Input Voltage, EN to GND	-0.3 to 30	
V_{CSx}	Output current sinks CS1 – CS16 to GND	-0.3 to 35	
V_{CC}	Low Voltage Pin to GND	-0.3 to 6.0	
OVP, COMP, SYNC, VSYNC, GSCLK, RSET, SDI, SDO, SCLK, CS B, PLL, FLAUT, CSFB, CSFBi, CSFBo, ADDR0, ADDR1	OVP, COMP, SYNC, VSYNC, GSCLK, RSET, SDI, SDO, SCLK, CS B, PLL, FLAUT, CSFB, CSFBi, CSFBo, ADDR0, ADDR1 Voltage to GND	-0.3 to V_{CC} + 0.3	
I_{OUT}	Maximum DC Output Current[2]	1800	mA
T_J	Maximum Junction Operating temperature	-40 to +150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	

Thermal Information[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance[4]	23	°C/W
P_D	Maximum Power Dissipation	4.3	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Based on long-term current density limitation.
3. Mounted on an FR4 board.
4. Derate 23mW/°C above 25°C.

Electrical Characteristics[1]

V_{IN}=24V; C_{IN} = 4.7µF, C_{OUT} = 4.7µF; C_{VCC} = 2.2µF; L_1 = 10µH; R_{SET} =10.2kΩ (I_{CSx} = 60mA); T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply, Current Sinks						
V_{IN}	Input Voltage Range		10.8		28.0	V
V_{UVLO}	Under-Voltage Threshold	V_{IN} Rising			10	V
		Hysteresis		500		mV
		V_{IN} Falling	8.5			V
V_{OUT}	Output Voltage Range	V_{IN} = 10.8 to 28.0V	V_{IN} + 3V		40	V
I_{Q_2402M}	Quiescent Current of AAT2402M (no switching)	I_{CSx} = 0mA, V_{CSx} = 1V		3		mA
I_{Q_2402S}	Quiescent Current of AAT2402S	I_{CSx} = 0mA, V_{CSx} = 1V		5		mA
I_{SD}	VIN Pin Shutdown Current	CSn = IN, EN = Logic Low; includes CSx + LX leakage current		25		µA
$I_{EN\_LEAKAGE}$	Enable Leakage Current	EN = 5V			5	µA
I_{ADDR0}, I_{ADDR1}	Input Current to ADDR0 and ADDR1	ADDR0 = 5V, ADDR1 = 5V			100	µA
V_{OVP}	Over-Voltage Threshold	V_{OUT} Rising	1.1	1.2	1.3	V
	Over-Voltage Hysteresis	V_{OUT} Falling		100		mV
$R_{DS(ON)LO}$	Low Side Switch On-Resistance			180		mΩ
I_{LIMIT}	Low Side Switch Current Limit		4.5		6.5	A
F_{OSC}	Oscillator Frequency		500	600	700	kHz
F_{SYNC}	Sync Frequency		300		900	kHz
T_{SS}	Soft-Start	V_{OUT} = 35V		1		ms
I_{CSx} / I_{RSET}	Current Set Ratio	I_{CSx}/I_{RSET}, V_{RSET} = 0.6V nom, Full Scale Dot Correction		1024		A/A
V_{Cx}	Current Sink Voltage	EN = Logic High, I_{CSx} = 60mA (R_{SET} = 10.2kΩ)		0.8		V
I_{CSx}	Current Sink Accuracy	I_{CSx} = 60mA	-2.5		+2.5	%
$I_{CSx\text{-}Matching}$	Current Matching Between Any Sink Channel	I_{CSx}= 60mA	-2		+2	%
$V_{Cx(SHORT)}$	Shorted Diode(s) Detection Threshold	I_{CSx}= 60mA		3		V
Logic Level Inputs: EN, SYNC, VSYNC, GSCLK, SDI, SCLK, CSB						
$V_{I(L)}$	Input Logic Threshold Low				0.4	V
$V_{I(H)}$	Input Logic Threshold High		1.4			V
$V_{I(H)\_EN}$	Enable Logic Threshold High		2.5			V

1. The AAT2402 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

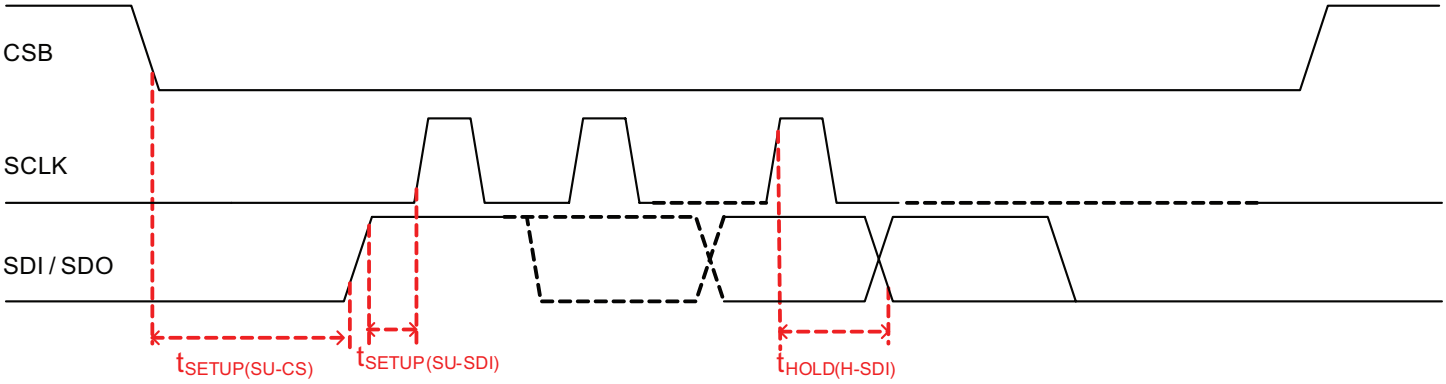
Electrical Characteristics[1]

V_{IN}=24V; C_{IN} = 4.7µF, C_{OUT} = 4.7µF; C_{VCC} = 2.2µF; L_1 = 4.2µH; R_{SET} =10.2kΩ (I_{CSx} = 60mA); T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Logic Level Outputs: SDO, FAULT						
VCCIO	VCC I/O Voltage Range	No Load	2.97	3.3	3.63	V
$V_{O(H)}$	Output Logic Level High	I_{SOURCE} = 4mA, V_{CCIO} = 3.3V	2.4			V
$V_{O(L)}$	Output Logic Level Low	I_{SINK} = -4mA			0.4	V
$V_{FAULTLOW}$	FAULT Logic Output Low				0.4	V
I_{SINK}	FAULT Logic Hi Leakage	V_{FAULT} = 5.5V			1	µA
Interface: VSYNC, GSCLK						
F_{VSYNC}	VSYNC Maximum Frequency		55		250	Hz
F_{GSCLK}	GSCLK Frequency			1		MHz
$t_{SETUP(SU\_VS)}$	Minimum VSYNC Setup Time	GSCLK, VSYNC		24		ns
$t_{HOLD(H\_VS)}$	Minimum VSYNC Hold Time	GSCLK, VSYNC		24		ns
$T_{GS(HI/LO\_MIN)}$	Minimum GSCLK Clock High/Low Time			32		ns
$t_{SCLK(HI/LO\_MIN)}$	Minimum SCLK Clock High/Low Time			32		ns
$t_{VS(HI/LO\_MIN)}$	Minimum VSYNC Clock High/Low Time			32		ns
SPI Interface: SDI, SDO, SCLK, CSB						
F_{MAX}	Maximum Clock Frequency			30		MHz
$t_{SETUP(SU\_SDI)}$	Minimum SDI Setup Time	SDI, SCLK		24		ns
$t_{SETUP(SU\_CS)}$	Minimum CSB Setup Time	CSB, SDI		24		ns
$t_{HOLD(H\_SDI)}$	Minimum SDI Hold Time	SDI, SCLK		24		ns
Thermal Protection						
$T_{J2(SD)}$	T_J Thermal Shutdown Threshold	Reset Thermal Threshold		140		°C
$T_{J2(HYS)}$	T_J Thermal Shutdown Hysteresis	CTL1 and CTL2 Registers are Reset to 0		15		°C
$T_{J1(SD)}$	T_J Thermal Warning Threshold	Warning Thermal Threshold		120		°C
$T_{J1(HYS)}$	T_J Thermal Warning Hysteresis			15		°C

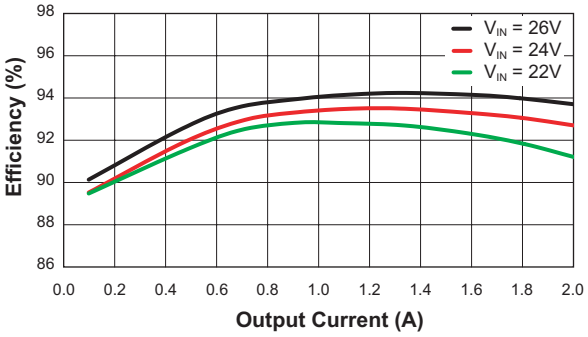
1. The AAT2402 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

SPI Timing Diagram

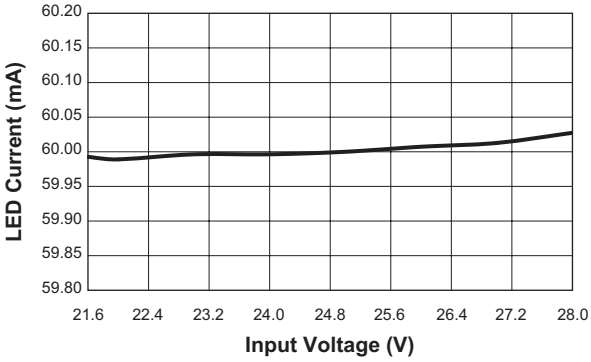


Typical Characteristics

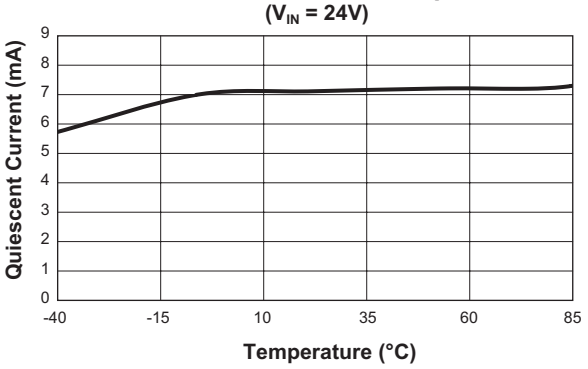
AAT2402M Boost Converter Efficiency vs. Output Current
(V_{OUT} = 38V)



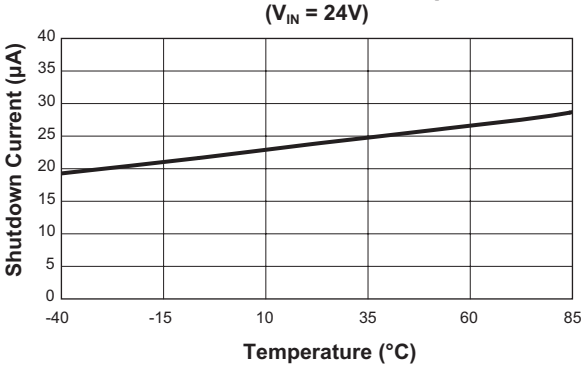
LED Current vs. Input Voltage
(60mA/ch)



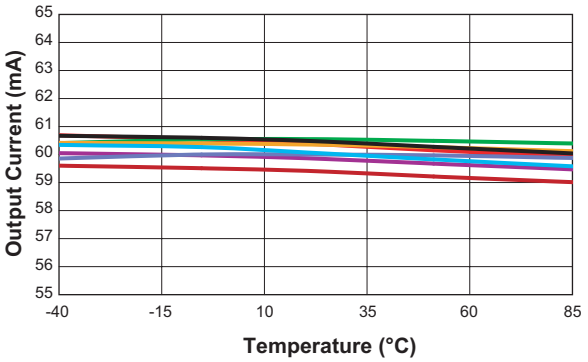
Sum of AAT2402M and AAT2402S Quiescent Current vs. Temperature
(V_{IN} = 24V)



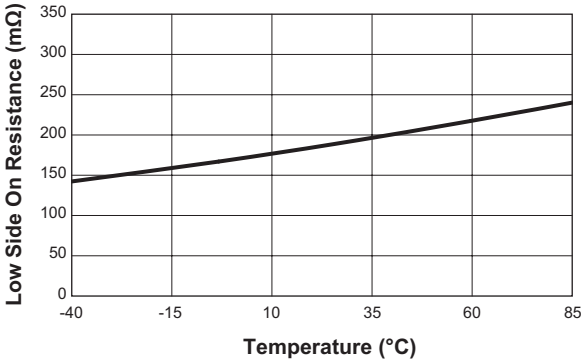
Sum of AAT2402M and AAT2402S Shutdown Current vs. Temperature
(V_{IN} = 24V)



Output Current Matching vs. Temperature
(60mA/ch)

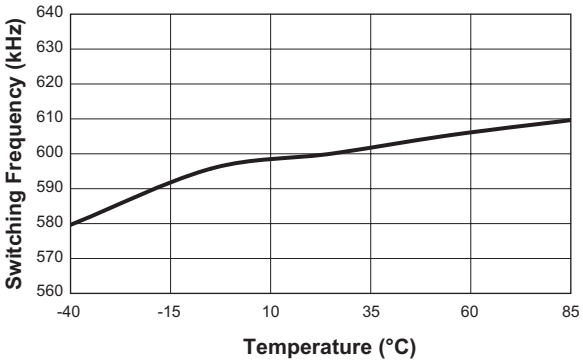


AAT2402M Boost Converter Low Side On-Resistance vs. Temperature

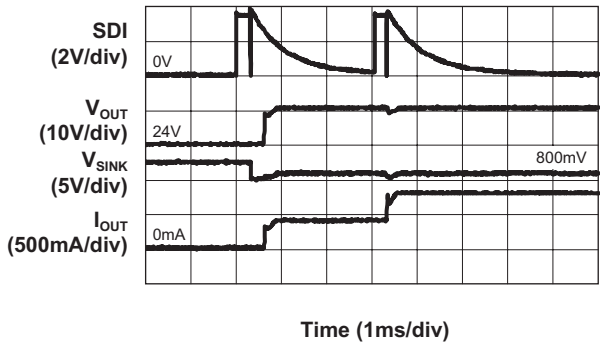


Typical Characteristics

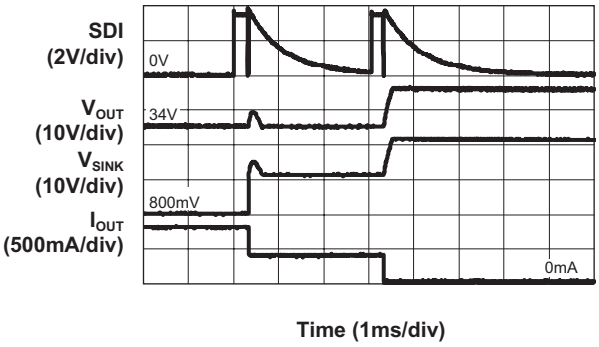
Switching Frequency vs. Temperature



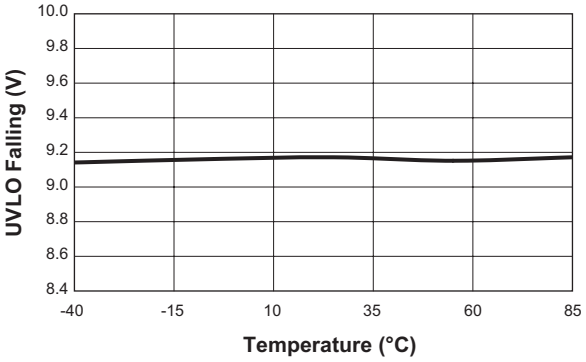
Turn On
(V_{IN} = 24V; 50mA/ch)



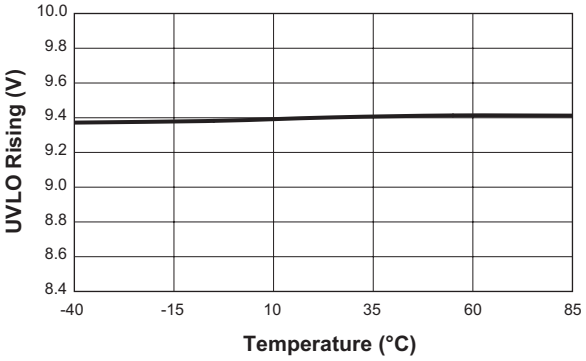
Turn Off
(V_{IN} = 24V; 50mA/ch)



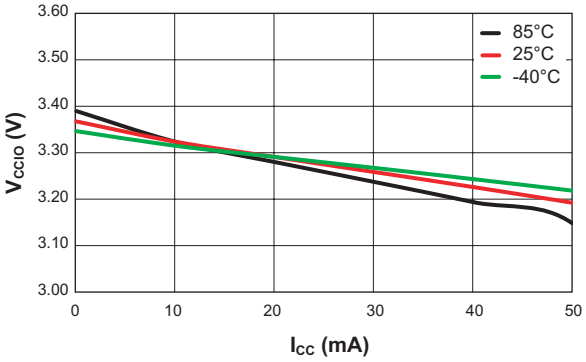
UVLO Falling vs. Temperature



UVLO Rising vs. Temperature

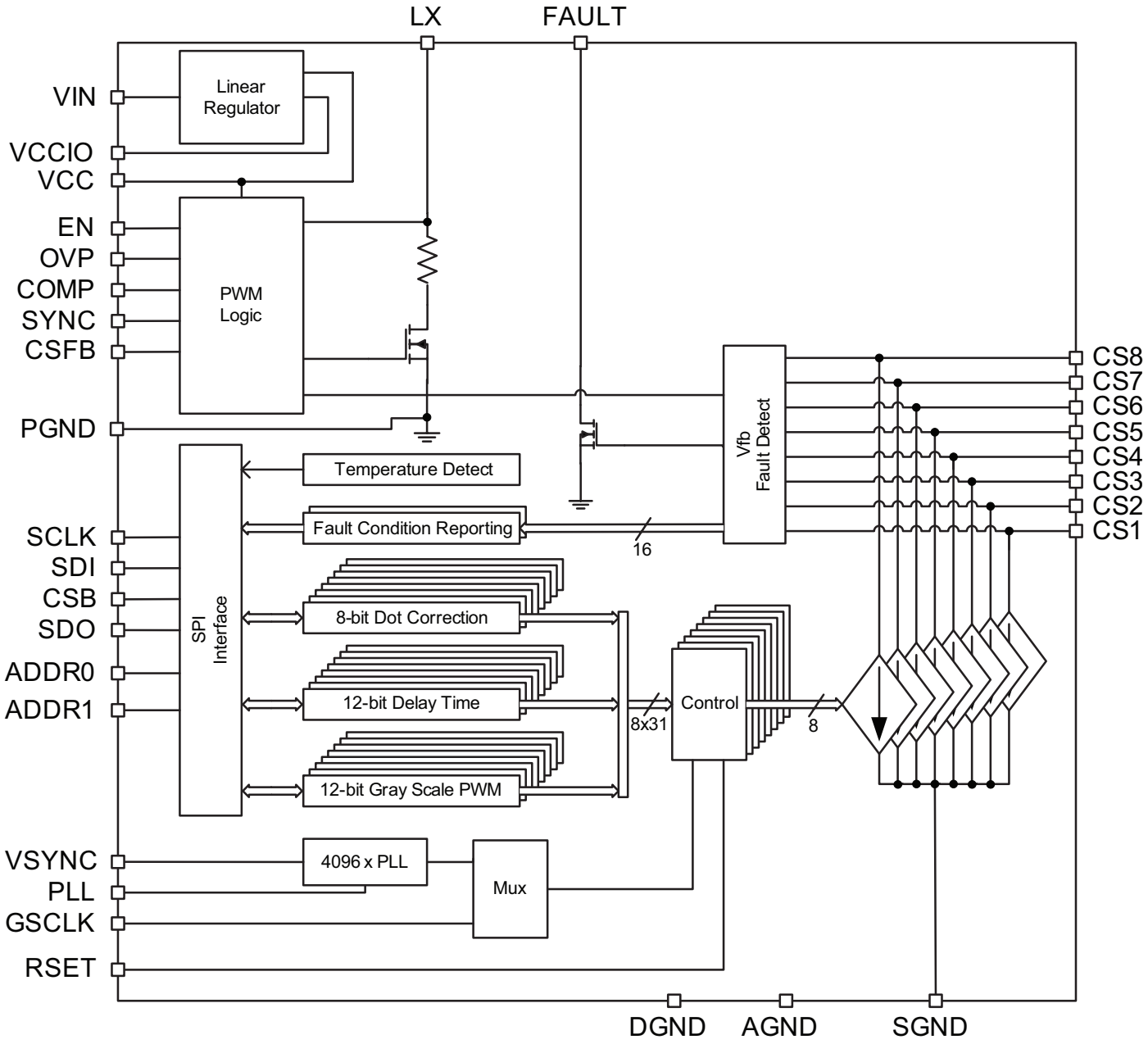


V_{CCIO} vs. I_{VCCIO}
(V_{IN} = 12V)

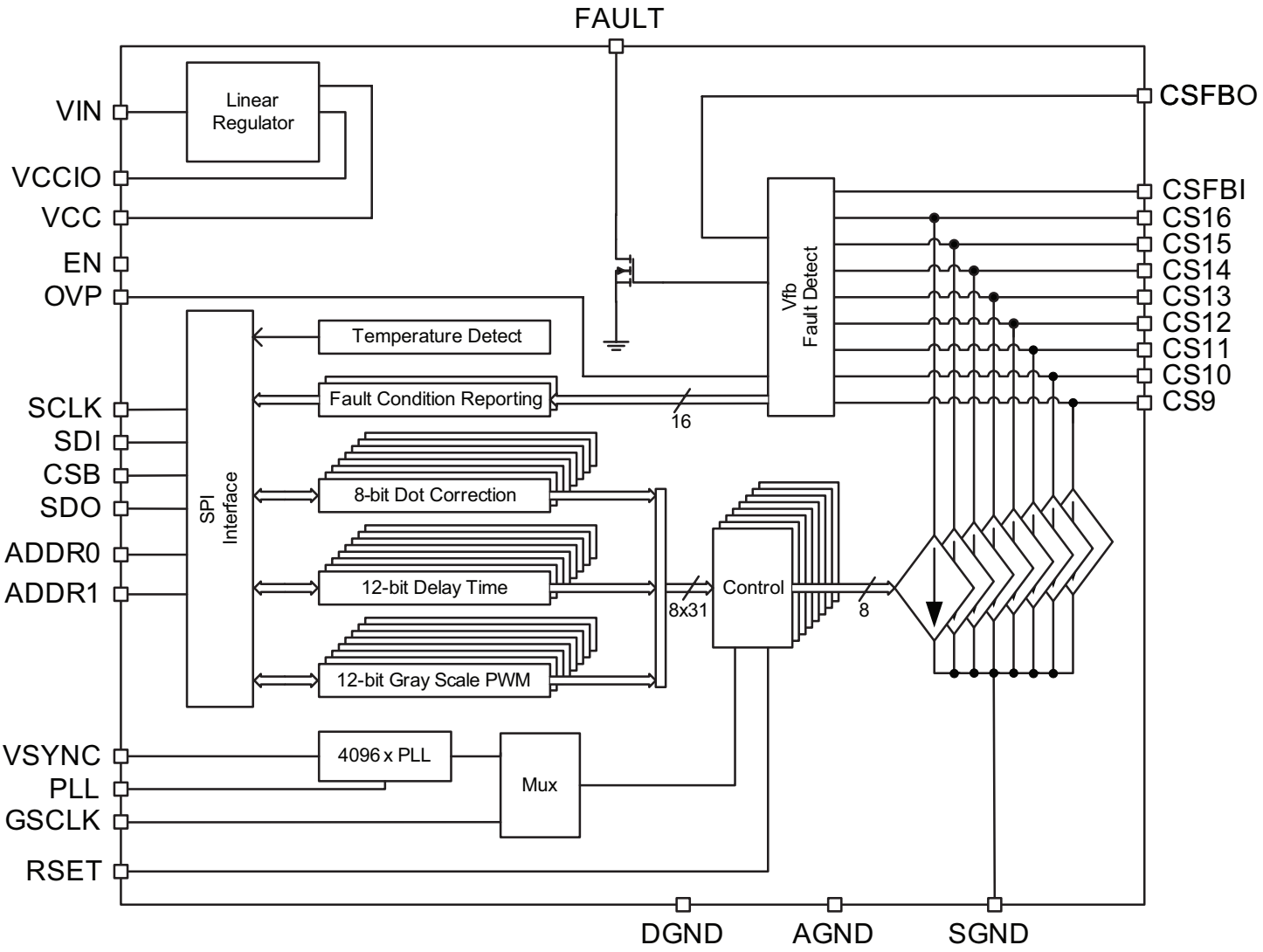


Functional Block Diagram

AAT2402M (master)



AAT2402S (slave)



Functional Description

The AAT2402M consists of a high efficiency DC/DC boost controller, an integrated slew rate controlled input disconnect MOSFET switch, and a MOSFET power switch. A high voltage rectifier, power inductor, output capacitor, feedback compensation network, and OVP resistor divider network are required to implement a DC/DC boost converter.

The AAT2402M's boost controller is designed to deliver 1600mA up to 40V. It can drive a total of 16 current regulated sinks (8 of its own and 8 from AAT2402S) with 10 HB white LEDs connected in series at each channel.

The maximum LED sink current can be set by an external resistor. Each current sink can be programmed through the SPI interface. Each sink allows independent control with different registers (DOT correction, Gray Scale, Delay, On/Off control configuration).

The AAT2402M and AAT2402S both provide one linear regulator for VCCIO supply.

Control Loop

The AAT2402M provides the benefits of current mode control with a simple feedback loop. The device maintains exceptional DC regulation, transient response, and cycle-by-cycle current limit with additional RC compensation components. The AAT2402M modulates the power MOSFET switching current in response to changes in output voltage (LED voltage). This allows the voltage loop to directly program the required inductor current in response to changes in the output load. The switching cycle initiates when the N-channel MOSFET is turned ON and current ramps up in the inductor. The ON interval is terminated when the feedback signal crossover the falling edge of the saw wave from the PWM modulator. During the OFF interval, the inductor discharges the energy (inductor ramps down) until the lower threshold, or zero inductor current, is reached. The lower current is equal to the peak current minus a preset hysteresis threshold which determines the inductor ripple current. The peak current is adjusted by the controller until the output current requirement is met. The magnitude of the feedback error signal determines the average input current. Therefore, the AAT2402M controller implements a programmed current source connected to the output capacitor and load resistor. There is no right-half plane zero, and loop stability is achieved with simple RC compensation components.

Soft Start / Enable

The input disconnect switch is activated when a valid supply voltage is present and the EN/SET pin is strobed high. Slew rate control on the input disconnect switch ensures minimal inrush current as the output voltage is charged to the input voltage, prior to switching of the N-channel power MOSFET. A monotonic turn-on is guaranteed by the built-in soft-start circuitry, which eliminates output current overshoot across the full input voltage range and over all load conditions.

Current Limit and Over-Temperature Protection

The switching of the N-channel MOSFET terminates when a current limit of 6.5A (max) is exceeded. This minimizes power dissipation and component stresses under overload and short-circuit conditions. Switching resumes when the current decays below the current limit. Thermal protection disables the AAT2402M/AAT2402S when the internal power dissipation causes the junction temperature to reach the thermal limit threshold (140°C, nominal). When the thermal threshold is reached, the control register, CTL1 or CTL2, is reset to 00h and all current sinks are disabled. When the AAT2402M's thermal threshold is reached, the boost converter is also disabled.

Over-Voltage Protection

Over-voltage protection prevents damage to the AAT2402M during open-circuit on any LED channel sinks causing high output voltage conditions. An overvoltage event is defined as a condition where the voltage on the OVP pin exceeds the over-voltage threshold limit (V_{OVP} = 1.2V typical). When the voltage on the OVP pin has reached the threshold limit, the converter stops switching and the output voltage decays. Switching resumes when the voltage on the OVP pin drops below the lower hysteresis limit, maintaining an average output voltage between the upper and lower OVP thresholds multiplied by the resistor divider scaling factor.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the V_{IN} input. Under-voltage lockout (UVLO) guarantees sufficient VIN bias and proper operation of all internal circuitry prior to soft start.

Current Sink Control

Each current sink has an independent property programmed by the following registers. The AAT2402M contains current sinks 1 through 8. The AAT2402S contains current sinks 9 through 16.

Dot Correction

Each current sink can have a separate current setting to compensate for relative LED brightness. A secondary latch holds the data until the rising edge of V_{SYNC}. After the rising edge of V_{SYNC}, the data in the DOT register takes effect. This register has a default setting of 0h.

ADDR: 00h to 1Eh		DOTn: DOT Correction Current Setting		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	DOTn 7:0	00h	R/W	8-bit DOT word

Table 1: DOT Correction Current Setting.

Gray Scale

Each current sink has a unique PWM duty cycle setting to provide a given brightness. The gray scale register is a 12-bit word divided into segments of 8 bits and 4 bits. A secondary latch holds the data until the falling edge of the associated PWM signal. In other words, the data is held until the associated LED current source turns off. At that time, the data in the SPI register takes effect. This register has a default setting of 0h. Only even register addresses are used starting from 40h to 7Eh.

ADDR: 40h to 7Eh		GSn LSB: Gray Scale Setting LSB		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	GSn 7:0	00h	R/W	8 LSBs of 12-bit GS word

Table 2: Gray Scale Setting LSB.

ADDR: 40h to 7Eh		GSn MSB: Gray Scale Setting MSB		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:0	GSn 11:8	00h	R/W	4 MSBs of 12-bit GS word

Table 3: Gray Scale Setting MSB.

Delay

Each current sink has a unique delay time from the start of V_{SYNC} to when the current sink PWM cycle begins. The delay register is a 12-bit word divided into segments of 8 bits and 4 bits. A secondary latch holds the data until the falling edge of the associated PWM signal. In other words, the data is held until the associated LED current source turns off. At that time, the data in the SPI register takes effect.

This register has a default setting of 0. Only even register addresses are used. Starting from 80h, every other even register is programmed up to BEh.

ADDR: 80h to BEh		DLYn LSB: Delay Setting LSB		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	DLYn 7:0	00h	R/W	8 LSBs of 12-bit GS word

Table 4: Delay Setting LSB.

ADDR: 80h to BEh		DLYn MSB: Delay Setting MSB		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:0	DLYn 11:8	00h	R/W	4 MSBs of 12-bit GS word

Table 5: Delay Setting MSB.

Current Sink ON/OFF

Each current sink can be independently enabled or disabled. In the event of an over temperature condition, this register is reset to 00h and must be reprogrammed to resume operation. It has a default setting of 00h (all sinks are off). A secondary latch holds the data until the rising edge of V_{SYNC}. After the rising edge of V_{SYNC}, the data in the DOT register takes effect.

ADDR: C0h		CTL1: This Register Enables or Disables Each Current Sink Independently		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	CS8:CS1	00h	R/W	0 = current sink OFF, 1= current sink ON

Table 6: CTL1 Setting.

ADDR: C2h		CTL2: This Register Enables or Disables Each Current Sink Independently		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	CS16:CS9	00h	R/W	0 = current sink OFF, 1= current sink ON

Table 7: CTL2 Setting.

PWM Timing

The PWM "on time" of a given current sink is set by the gray scale and delay registers according to the following timing diagram. T_{VSYNC} is the period of the V_{SYNC} signal, typically 1/120 Hz, or 8 1/3 ms, but T_{VSYNC} can be as short as 500µs. GSCLK is either derived from V_{SYNC}, where F_{GSCLK} = 4096 x F_{VSYNC}, or supplied by an external signal at the GSCLK pin. T_{DLY} is the number between 0 and 4095 of the DLY register, and is the number of GSCLK rising edges between the rising edge of V_{SYNC} and the rising edge of the PWM signal. Likewise, T_{PWM} is the number between 0 and 4095 of the GS register, and is the number of GSCLK periods of the PWM "on time". The current sink conducts during the PWM "on time" (shown high in the following timing diagram). If T_{PWM} is not met by the end of T_{VSYNC}, the PWM on time will overflow onto the next T_{VSYNC} period. LED % Brightness = T_{PWM} /4096 x 100.

Device Address Setup

The device address is set by the two address pins, ADDR1 and ADDR0. Each address pin has four decode levels resulting in 16 possible address settings. The address is programmed by connecting ADDR1 and ADDR0 to VCC, GND, SDI, or by leaving the ADDR pin unconnected. The master and slave devices can be programmed with the same device address. The register addressing will automatically select the appropriate master/slave device for the addressed current sink.

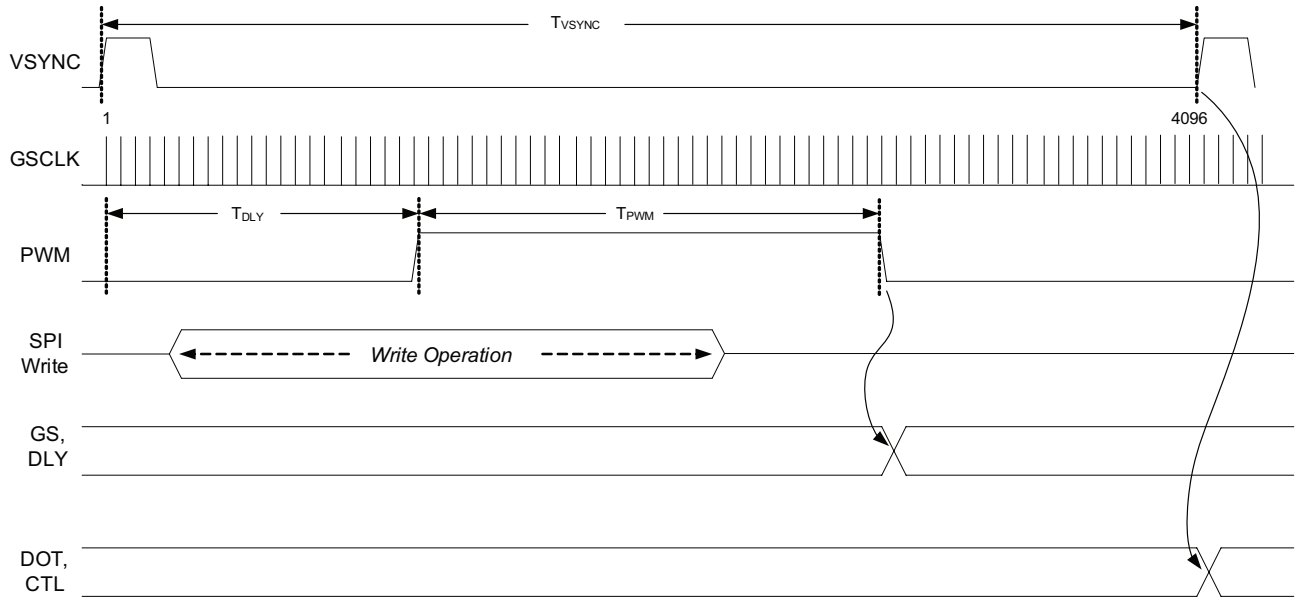


Figure 1: PWM Timing Diagram.

Device Address		SPI Address: Addr1 Addr0 Decoding of Address Set Resistors
Bit	**Bit Name**	**Description**
1:0	ADDR0	00: connect to VCC; 01: OPEN; 10: connect to SDI; 11: connect to GND
3:2	ADDR1	00: connect to VCC; 01: OPEN; 10: connect to SDI; 11: connect to GND

Table 8: Device Address Settings.

Configuration		Bits								
ADDR1	ADDR0	6	5	4	3	2	1	0	W	Address (Hex)
VCC	VCC	1	0	1	0	0	0	0	0	A0
VCC	OPEN	1	0	1	0	0	0	1	0	A2
VCC	SDI	1	0	1	0	0	1	0	0	A4
VCC	GND	1	0	1	0	0	1	1	0	A6
OPEN	VCC	1	0	1	0	1	0	0	0	A8
OPEN	OPEN	1	0	1	0	1	0	1	0	AA
OPEN	SDI	1	0	1	0	1	1	0	0	AC
OPEN	GND	1	0	1	0	1	1	1	0	AE
SDI	VCC	1	0	1	1	0	0	0	0	B0
SDI	OPEN	1	0	1	1	0	0	1	0	B2
SDI	SDI	1	0	1	1	0	1	0	0	B4
SDI	GND	1	0	1	1	0	1	1	0	B6
GND	VCC	1	0	1	1	1	0	0	0	B8
GND	OPEN	1	0	1	1	1	0	1	0	BA
GND	SDI	1	0	1	1	1	1	0	0	BC
GND	GND	1	0	1	1	1	1	1	0	BE

Table 9: Device Address Write Table and Configuration.

Configuration		Bits								
ADDR1	ADDR0	6	5	4	3	2	1	0	R	Address (Hex)
VCC	VCC	1	0	1	0	0	0	0	1	A1
VCC	OPEN	1	0	1	0	0	0	1	1	A3
VCC	SDI	1	0	1	0	0	1	0	1	A5
VCC	GND	1	0	1	0	0	1	1	1	A7
OPEN	VCC	1	0	1	0	1	0	0	1	A9
OPEN	OPEN	1	0	1	0	1	0	1	1	AB
OPEN	SDI	1	0	1	0	1	1	0	1	AD
OPEN	GND	1	0	1	0	1	1	1	1	AF
SDI	VCC	1	0	1	1	0	0	0	1	B1
SDI	OPEN	1	0	1	1	0	0	1	1	B3
SDI	SDI	1	0	1	1	0	1	0	1	B5
SDI	GND	1	0	1	1	0	1	1	1	B7
GND	VCC	1	0	1	1	1	0	0	1	B9
GND	OPEN	1	0	1	1	1	0	1	1	BB
GND	SDI	1	0	1	1	1	1	0	1	BD
GND	GND	1	0	1	1	1	1	1	1	BF

Table 10: Device Address Read Table and Configuration.

Fault Reporting

Each device possesses fault reporting registers and a fault flag. An open or short condition on each current sink is reported in one of four fault registers. An open fault condition is only monitored for LED current sink on-times of greater than 10µs. An over-temperature condition is reported in one of two registers. These conditions may selectively be reported on the open drain Fault pin. Bits in separate fault reporting registers can be set or reset to enable or disable a particular fault condition.

The shorted LED fault condition is handled in a special way because of the uncertainty associated with shorted LEDs and the LED forward voltage variation. To detect a shorted LED fault in the system, all LED channels should be programmed to be conducting for at least 1ms. The fault flag will only be valid 1ms after a given LED string has begun conducting. If the fault flag becomes active, the fault registers must be read while the channels remain conducting. The fault reporting register defaults to the condition of reporting the short detect, so this register must be cleared prior to checking for shorted LEDs. Severe LED forward voltage (V_F) mismatches between channels will also be reported as a short fault condition with the lower V_F channels indicating the fault condition.

Fault Registers

The fault registers can be read at any time during operation.

ADDR: E0h		Fault1: This Register Reports Fault Conditions And High Voltage CS Pins		
Bit	Bit Name	Default	Access	Description
1:0	CS1 Fault	00h	R	00: no fault, 01: open, 10: short
3:2	CS2 Fault	00h	R	00: no fault, 01: open, 10: short
5:4	CS3 Fault	00h	R	00: no fault, 01: open, 10: short
7:6	CS4 Fault	00h	R	00: no fault, 01: open, 10: short

Table 11: Fault1 Register Settings.

ADDR: E2h		Fault2: This Register Reports Fault Conditions and High Voltage CS Pins		
Bit	Bit Name	Default	Access	Description
1:0	CS5 Fault	00h	R	00: no fault, 01: open, 10: short
3:2	CS6 Fault	00h	R	00: no fault, 01: open, 10: short
5:4	CS7 Fault	00h	R	00: no fault, 01: open, 10: short
7:6	CS8 Fault	00h	R	00: no fault, 01: open, 10: short

Table 12: Fault2 Register Settings.

ADDR: E4h		Fault3: This Register Reports Fault Conditions And High Voltage CS Pins		
Bit	Bit Name	Default	Access	Description
1:0	CS9 Fault	00h	R	00: no fault, 01: open, 10: short
3:2	CS10 Fault	00h	R	00: no fault, 01: open, 10: short
5:4	CS11 Fault	00h	R	00: no fault, 01: open, 10: short
7:6	CS12 Fault	00h	R	00: no fault, 01: open, 10: short

Table 13: Fault3 Register Settings.

ADDR: E6h		Fault4: This Register Reports Fault Conditions and High Voltage CS Pins		
Bit	Bit Name	Default	Access	Description
1:0	CS13 Fault	00h	R	00: no fault, 01: open, 10: short
3:2	CS14 Fault	00h	R	00: no fault, 01: open, 10: short
5:4	CS15 Fault	00h	R	00: no fault, 01: open, 10: short
7:6	CS16 Fault	00h	R	00: no fault, 01: open, 10: short

Table 14: Fault4 Register Settings.

Temperature Fault Conditions

Two thermal limits are reported in each AAT2402M/2402S device. The first thermal limit serves as a warning that the device is heating up. When this condition is reported, the system can compensate by lowering the current levels of the current sinks. The second thermal limit is the maximum temperature allowed. When this temperature is reached, the control registers are reset to 0 which disables all current sinks. In addition, the boost converter in the master device is disabled. To resume operation, the control registers must be reset, and all of the configuration registers must be reprogrammed, since data retention at the maximum temperature is not guaranteed.

ADDR: E8h		OTMP1: Reports the Temperature Condition of the Master IC (CS8 to CS1)		
Bit	Bit Name	Default	Access	Description
1:0	OTMP 1	00h	R	00: Tj < T1 01: T1 < Tj < T2 11: T2 < Tj
2	Config	0h	R/W	0: Report T1 and T2 Thermal Limits on Fault pin 1: Report only T2 Thermal Limit on Fault pin

Table 15: OTMP1 Settings.

ADDR: EAh		OTMP2: Reports the Temperature Condition of the Slave IC (CS16 to CS9)		
Bit	Bit Name	Default	Access	Description
1:0	OTMP 2	00h	R	00: Tj < T1 01: T1 < Tj < T2 11: T2 < Tj
2	Config	0h	R/W	0: Report T1 and T2 Thermal Limits on Fault pin 1: Report only T2 Thermal Limit on Fault pin

Table 16: OTMP2 Settings.

Fault Reporting Registers

Each individual sink's fault reporting can be configured to the following cases: LED string becomes open, LED string becomes short completely, reporting both or report none. To turn this feature off, set two bits to '11'. Setting the two bits to '01' and '10' means reporting short condition only or reporting open condition only accordingly. To report both faulty conditions, set the two bits to '00'.

ADDR: F0h		Fault Reporting 1: Individual Sink Fault Reporting		
Bit	Bit Name	Default	Access	Description
1:0	CS1 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
3:2	CS2 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
5:4	CS3 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
7:6	CS4 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.

Table 17: Fault Reporting Register 1 Settings.

ADDR: F2h		Fault Reporting 2: Individual Sink Fault Reporting		
Bit	Bit Name	Default	Access	Description
1:0	CS5 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
3:2	CS6 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
5:4	CS7 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
7:6	CS8 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.

Table 18: Fault Reporting Register 2 Settings.

ADDR: F4h		Fault Reporting 3: Individual Sink Fault Reporting		
Bit	Bit Name	Default	Access	Description
1:0	CS9 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
3:2	CS10 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
5:4	CS11 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
7:6	CS12 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.

Table 19: Fault Reporting Register 3 Settings.

ADDR: F6h		Fault Reporting 4: Individual Sink Fault Reporting		
Bit	Bit Name	Default	Access	Description
1:0	CS13 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
3:2	CS14 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
5:4	CS15 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.
7:6	CS16 Fault	10h	R/W	00: report both; 01: report short only; 10: report open only; 11: report none.

Table 20: Fault Reporting Register 4 Settings.

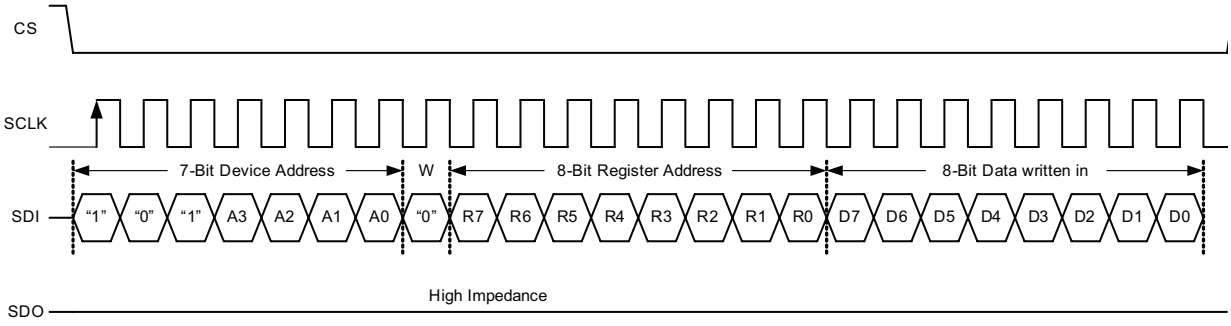
Serial Peripheral Interface (SPI)

The serial peripheral interface is a synchronous serial interface for address and data transfer at bit rates of up to 30Mhz. It is configured in 8-bit bytes designed to interface with a standard SPI bus on many microcontrollers. Four pins are used to communicate on the SPI: SCLK (synchronous clock), CS (chip select, to signify the start of a transfer), SDI (data input to the AAT2402M/2402S for write operations, latched on the rising edge of SCLK), and SDO (data output from the AAT2402M/2402S for read operations, presented on the falling edge of SCLK).

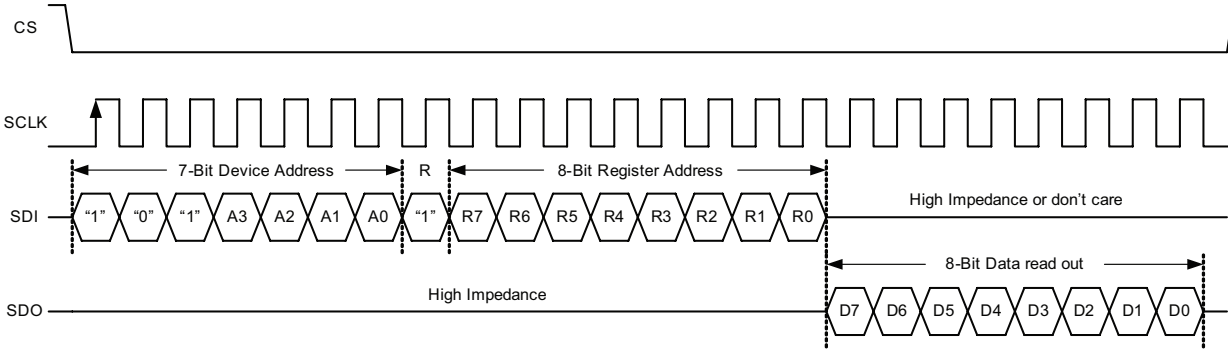
Data and address are always sent MSB first. The first 8-bit byte of a transfer is always the device address. The second byte of a transfer is always the address of the register to be written to or read from. The subsequent bytes are one or more bytes of data. The LSB (bit 0) of the device address byte contains a bit that signifies a read or a write operation. If R/W is 0, one or more write cycles occur, and if R/W is 1, one or more read cycles occur.

Multi-byte transfers are similar to single byte transfers, except that the CS pin is held low, and additional SCLK cycles are sent until the end of the burst. In multi-byte transfers, the registers are written to or read from in sequential order. After the end of the address space, the multi-byte transfer is terminated.

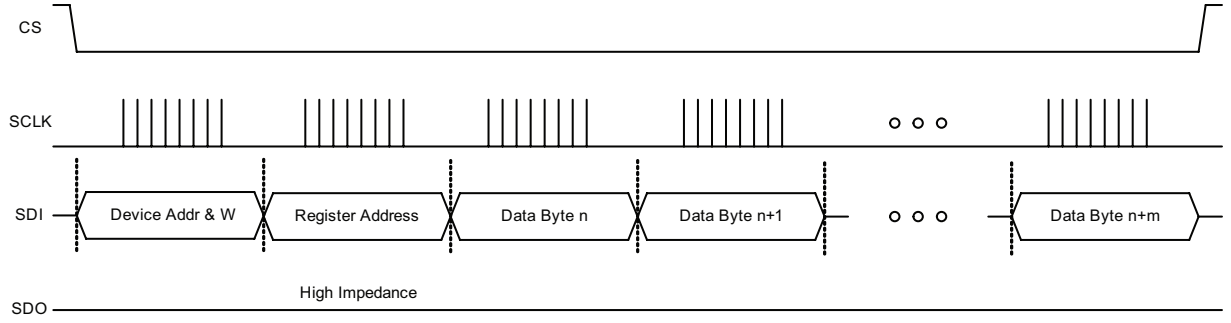
SPI Single-Byte Write



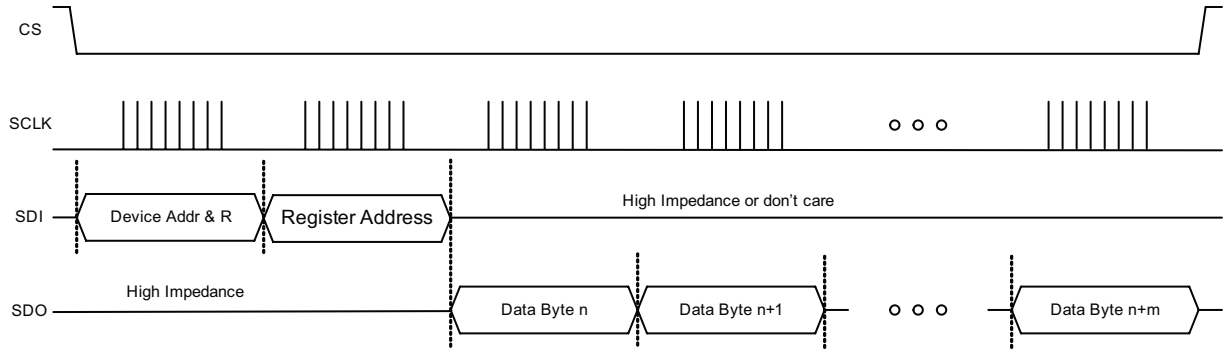
SPI Single-Byte Read



SPI Multi-Byte Write Transfer



SPI Multi-Byte Read Transfer



Application Information

Channel Disable

If current sink channels on either the AAT2402M or AAT2402S are not used, they must be terminated. Unused channels should have their corresponding bit in the CTL1 or CTL2 register set to zero. In applications where the AAT2402M/AAT2402S pair are used, unused channels may be tied to GND or to VCC. In applications where the AAT2402S is used alone, unused channels must be tied to VCC.

LED Selection

Although the AAT2402M and 2402S are specifically designed to drive high current white LEDs, the device can also be used to drive most types of LEDs with forward voltages ranging between 2.0V and 4.7V. Since all current sinks are matched with low voltage dependence, the LED-to-LED brightness will be matched regardless of the individual LED forward voltage (V_F) levels. It makes the AAT2402M and 2402S a perfect combination for large LCD TV backlighting LED applications.

Constant Current Setting

The LED current is controlled by the R_{SET} resistor. For maximum accuracy, a 1% tolerance resistor is recommended. Table 21 shows the R_{SET} resistor value for the AAT2402M and 2402S for various LED full-scale current levels.

$$R_{SET} = \frac{1024(A/A) \cdot 0.6V}{I_{CSx}}$$

I_{CSX} (mA)	R_{SET} (kΩ)
40	15.4
50	12.3
60	10.2
70	8.76
80	7.68
90	6.81
100	6.12

Table 21: Maximum LED Current and R_{SET} Resistor Values (1% Resistor Tolerance).

Over-Voltage Protection

The over-voltage protection circuit consists of a resistor network connected from the output voltage to the OVP pin (see Figure 2). This over-voltage protection circuit prevents damage to the device when one of the 16 channels has an open LED circuit. The rest of the channels of AAT2402M and AAT2402S continue to operate.

The resistor divider can be selected such that the over-voltage threshold occurs prior to the output reaching 45V ($V_{OUT(MAX)}$). The value of R5 should be selected from 10kΩ to 20kΩ to minimize switching losses without degrading noise immunity.

$$R_4 = R_5 \left(\frac{V_{OUT(PROTECTION)}}{V_{OVP}} - 1 \right)$$

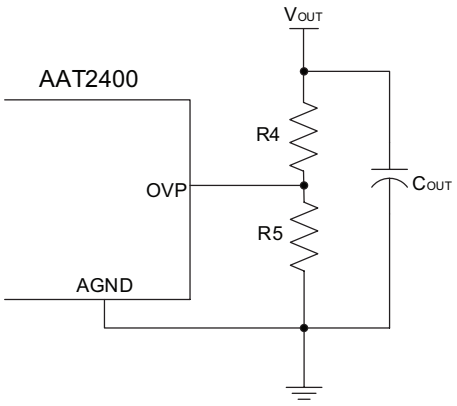


Figure 2: Over-Voltage Protection Circuit.

If 10 LEDs are connected in series on one channel sink, the total V_F from the WLEDs could be as high as 42V. Therefore, using R5 = 12.1kΩ and setting $V_{OUT(PROTECTION)}$ = 45V is recommended. Selecting a 1% resistor, this results in R4 = 442kΩ (rounded to the nearest standard 1% value). It is always recommended to use the same number of WLEDs on each channel and set the appropriate over-voltage protection. Failure to do so may cause any one of the 16 sink pins to exceed the absolute maximum rating voltage and permanently damage the device in case the channel is disconnected (open circuit failure).

LED Brightness Control

The AAT2402M and 2402S uses the SPI interface to program and control LED brightness. Each channel sink current of the AAT2402M and AAT2402S can be changed successively to brighten or dim the LED string in smooth transitions (i.e. dynamic local dimming or zone dimming), giving the user complete programmability and real-time control of LED brightness to tune the picture background to a true-black and a true-white from the LED technology.

Minimum and Maximum Practical Settings for Gray Scale and Delay Registers

When using the internally generated PLL derived PWM timebase, the stability of the frequency on V_{SYNC} defines the practical minimum and maximum settings for the gray scale and delay registers. As a rule, the minimum and maximum settings should be 4 counts away from full scale. In other words, the register settings should lie between 04h and 0FFBh. Otherwise, the natural phase delay between jitter on V_{SYNC} and the internal timebase may result in unexpected PWM timing. Gray scale set to zero, however, always results in zero on time.

Selecting the Schottky Diode

To ensure minimum forward voltage drop and no recovery, high voltage Schottky diodes are recommended for the AAT2402M boost converter. The output diode is selected to maintain acceptable efficiency and reasonable operating junction temperature under full load operating conditions. Forward voltage (V_F) and package thermal resistance (θ_{JA}) are the dominant factors in selecting a diode. The diode non-repetitive peak forward surge current rating (I_{FSM}) should be considered for high pulsed load applications. I_{FSM} rating drops with increasing conduction period.

Manufacturers' datasheets should be reviewed carefully to verify reliability under peak loading conditions. The diode's published current rating may not reflect actual operating conditions and should be used only as a comparative measure between similarly rated devices.

60V/3A rated Schottky diodes are recommended for output voltages less than 45V (total V_F and 100mA/sink application).

Estimating Schottky Diode Power Dissipation

The switching period is divided between ON and OFF time intervals:

$$\frac{1}{F_S} = t_{ON} + t_{OFF} = D + D'$$

During the ON time, the N-channel power MOSFET is conducting and storing energy in the boost inductor. During the OFF time, the N-channel power MOSFET is not conducting. Stored energy is transferred from the input battery and boost inductor to the output load through the output diode.

Duty cycle is defined as the ON time divided by the total switching interval:

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \cdot F_S$$

The maximum duty cycle can be estimated from the relationship for a continuous mode boost converter. Maximum duty cycle (D_{MAX}) is the duty cycle at minimum input voltage ($V_{IN(MIN)}$):

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

The average diode current during the OFF time can be estimated:

$$I_{AVG(OFF)} = \frac{I_{OUT}}{1 - D_{MAX}}$$

The V_F of the Schottky diode can be estimated from the average current during the off time. The average diode current is equal to the output current:

$$I_{AVG(TOT)} = I_{OUT}$$

The average output current multiplied by the forward diode voltage determines the loss of the output diode:

$$P_{LOSS(DIODE)} = I_{AVG(TOT)} \cdot V_F = I_{OUT} \cdot V_F$$

For continuous LED currents, the diode junction temperature can then be estimated:

$$T_{J(DIODE)} = T_{AMB} + \theta_{JA} \cdot P_{LOSS(DIODE)}$$

External Schottky diode junction temperature should be below 110°C, and may vary depending on application and/or system guidelines. The diode θ_{JA} can be minimized with additional metal PCB area on the cathode. However, adding additional heat-sinking metal around the anode may degrade EMI performance. The reverse leakage current of the rectifier must be considered to maintain low quiescent (input) current and high efficiency under light load. The rectifier reverse current increases dramatically at elevated temperatures.

Manufacturer	Part Number	Rated Foward Current (A)	Rated Voltage (V)	Thermal Resistance, θ_{JA}, (°C/W)	Case
Diode, Inc.	B360A	3A	60	100	SMA
ON Semi	MBRD360	3A	60	80	DPAK

Table 22: Typical Surface Mount Schottky Rectifiers for Various Output Loads (select T_J < 110°C in Application Circuit).

Selecting the Boost Inductor

The AAT2402M controller utilizes PWM control and the switching frequency is fixed. To maintain 600kHz switching frequency and stable operation, a 10µH inductor is recommended. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and peak inductor current rating, which is determined by the saturation characteristics. Measurements at full load and high ambient temperature should be performed to ensure that the inductor does not saturate or exhibit excessive temperature rise.

The output inductor (L) is selected to avoid saturation at minimum input voltage and maximum output load conditions. Worst-case peak current occurs at minimum input voltage (maximum duty cycle) and maximum load. At high load the switching frequency is somewhat diminished, resulting in higher I_{PEAK}. Bench measurements are recommended to confirm actual I_{PEAK} and to ensure that the inductor does not saturate at maximum LED current and minimum input supply voltage. The RMS current flowing through the boost inductor is equal to the DC plus AC ripple components. Under worst case RMS conditions, the current waveform is critically continuous. The resulting RMS calculation yields worst case inductor loss. The RMS current value should be compared against the inductor manufacturer's temperature rise, or thermal degrading, guidelines:

$$I_{RMS} = \frac{I_{PEAK}}{\sqrt{3}}$$

For a given inductor type, smaller inductor size leads to an increase in DCR winding resistance and, in most cases, increased thermal impedance. Winding resistance degrades boost converter efficiency and increases the inductor's operating temperature:

$$P_{LOSS(L)} = I^2_{RMS} \cdot DCR$$

Manufacturer	Part Number	Inductance (µH)	Saturated Rated Current (A)	DCR (mΩ)	Size (mm) LxWxH	Type
Cooper Bussmann	DR1040-100-R	10	4.4	26	10.3 x 10.5 x 4.0	Shielded Drum Core
Cooper Bussmann	DR1050-100-R	10	4.58	18	10.3 x 10.5 x 5.0	Shielded Drum Core
Sumida	CDR12D43RNP-100M	10	6.3	18	12.4 x 12.4 x 4.5	Shielded Drum Core
Sumida	CDR10D48MNNP-100MC	10	5.5	32	10.3 x 10.3 x 5.0	Shielded Drum Core
Sumida	CDRH10D43RNP-100NC	10	5.2	26.1	10.5 x 10.8 x 4.5	Shielded Drum Core
Sumida	CDRH105RNP-100NC	10	4.45	26	10.3 x 10.5 x 5.0	Shielded Drum Core
TDK	VLF10045T-100M4R3-PF	10	4.3	25	9.7 x 10.0 x 4.5	Shielded Drum Core
TDK	RLF12545T-100M5R1-PF	10	6	12.4	12.8 x 12.5 x 4.7	Shielded Drum Core
Würth Elektronik	WE-PD Type "LS" - 100	10	4.2	25	12 x 12 x 4.5	Shielded Drum Core

Table 23: Typical Suggested Surface Mount Inductors.

AAT2402M/2402S Input Capacitors

In general, it is good design practice to place a decoupling capacitor (input capacitor) between the IN and GND pins. An input capacitor in the range of 2.2µF to 10µF is recommended. A larger input capacitor in this application may be required for stability and transient response.

Multi-layer ceramic (MLC) capacitors provide small size and adequate capacitance, low parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL). MLC capacitors of type X7R or X5R are good to ensure capacitance stability over the full operating temperature range.

Boost Converter Output Capacitor Selection

For best performance, a low-ESR aluminum electrolytic type capacitor is suggested for use with the AAT2402M boost converter output. Other capacitor dielectric types are compatible and may be used such as Polymer cathode tantalum chip capacitors or low ESR OS-CON (organic semiconductor) capacitors. The voltage rating for a selected capacitor should exceed the greatest operating output voltage for the AAT2402M boost converter. Best engineering practices would recommend a capacitor voltage rating of two times the maximum operating voltage, although any voltage rating above the maximum operating output voltage of the boost converter is acceptable.

PCB Layout Guidelines

Boost converter performance can be adversely affected by poor layout. Possible impact includes high input and output voltage ripple, poor EMI performance, and reduced operating efficiency. Every attempt should be made to optimize the layout in order to minimize parasitic PCB effects (stray resistance, capacitance, and inductance) and EMI coupling from the high frequency LX node. A suggested PCB layout for the AAT2402M boost converter is shown in Figures 4 and 7. The following PCB layout guidelines should be considered:

1. Minimize the distance from Capacitor C1 and C2's negative terminals to the PGND pins. This is especially true with output capacitor C2, which conducts high di/dt current from the output diode back to the PGND pins.
2. Minimize the distance between L1 to D1 and switching pin SW; minimize the size of the PCB area connected to the SW pin.
3. Maintain a ground plane and connect to the IC PGND pin(s) as well as the PGND connections of CIN and COUT.
4. Consider additional PCB metal area on D1's cathode to maximize heat sinking capability. This may be necessary when using a diode with a high V_F and/or thermal resistance.
5. Consider additional PCB exposed area for the AAT2402M to maximize heat sinking capability. This may be necessary when using high output voltage and high current with minimum input voltage application. Connect the exposed paddle (bottom of the die) to PGND or GND. Connect AGND, DGND to SGND as close as possible to the package and maximize the heat sinking space for overall.
6. To maximize package thermal dissipation and power handling capacity of the AAT2402M and AAT2402S TQFN55-36 package, solder the exposed paddle of the IC onto the thermal landing of the PCB, where the thermal landing is connected to the ground plane. If heat is still an issue, multi-layer boards with dedicated ground planes are recommended. Also, adding more thermal vias on the thermal landing would help transfer heat to the PCB effectively.

Manufacturer	Part Number	Capacitance (µF)	Voltage Rating (V)	Temp Co.	Case Size
Murata	GRM185R60J225KE26	2.2	6.3	X5R	0603
Murata	GRM188R71A225KE15	2.2	10	X7R	0603
Taiyo Yuden	JMK107BJ225KK-T	2.2	6.3	X7R	0603
Taiyo Yuden	LMK107BJ225KA-T	2.2	10	X7R	0603
Murata	GRM31CR61H225KA88L	2.2	50	X5R	1206
TDK	C3225X7R2A225K	2.2	100	X5R	1210
Murata	GRM31CR71H475KA12L	4.7	50	X5R	1206
Panasonic	EEV-HA1H2R2R	2.2uF	50V	Elect SMD	4x4x5.4
Sanyo	50CE4R7BE	2.2uF	50V	Elect SMD	4x4x5.4

Table 24: Typical Suggested Surface Mount Capacitors.

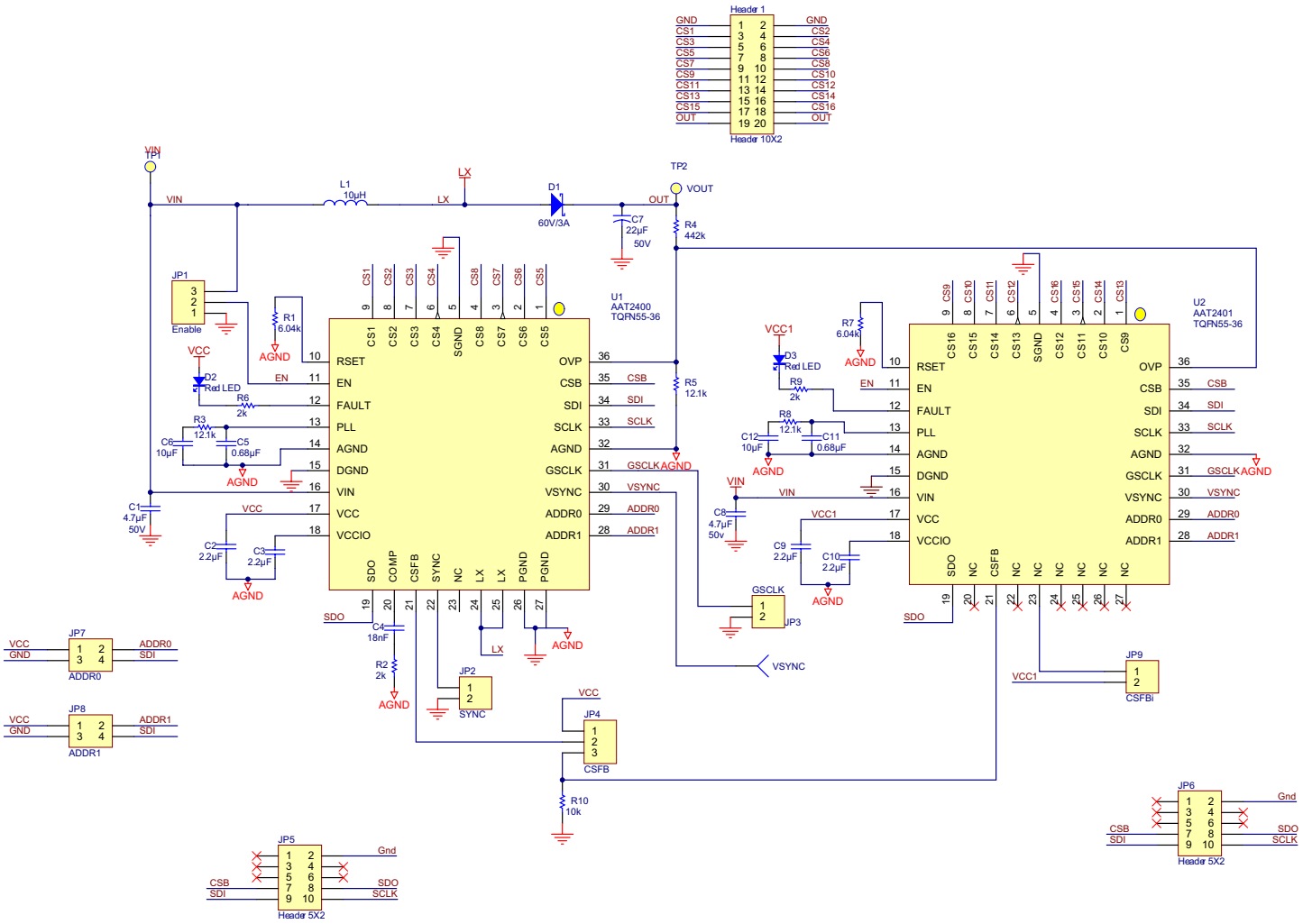


Figure 3: AAT2402M and AAT2402S DB1 Evaluation Board Schematic.

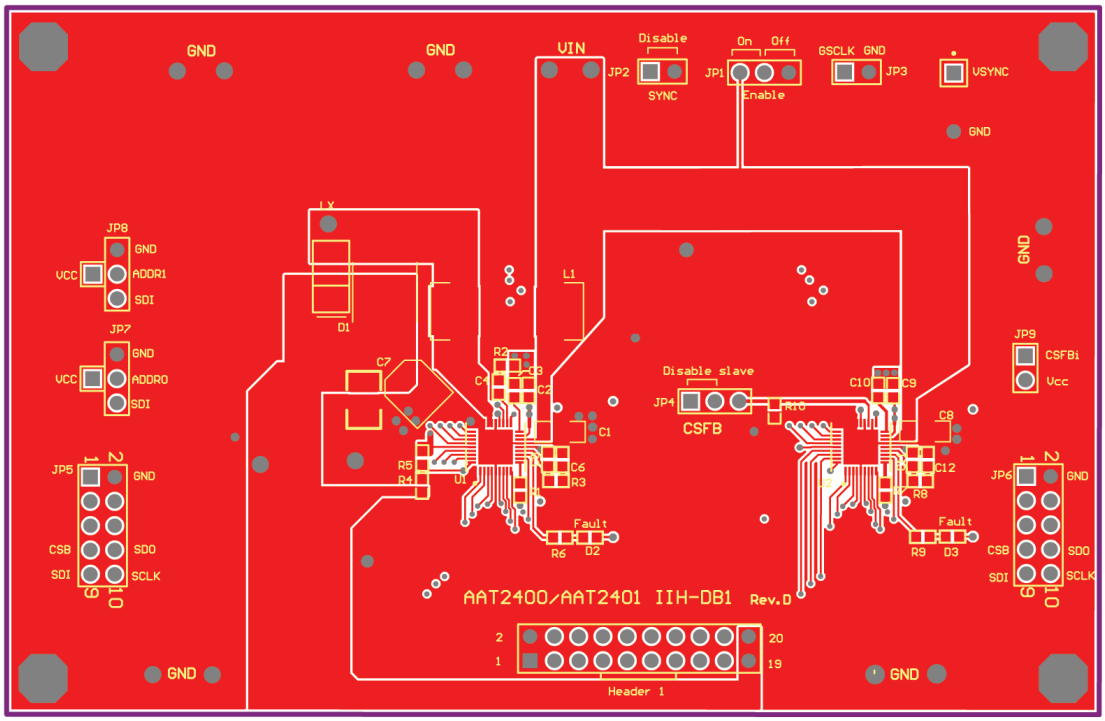


Figure 4: AAT2402M and AAT2402S Evaluation Board Top Side Layout.

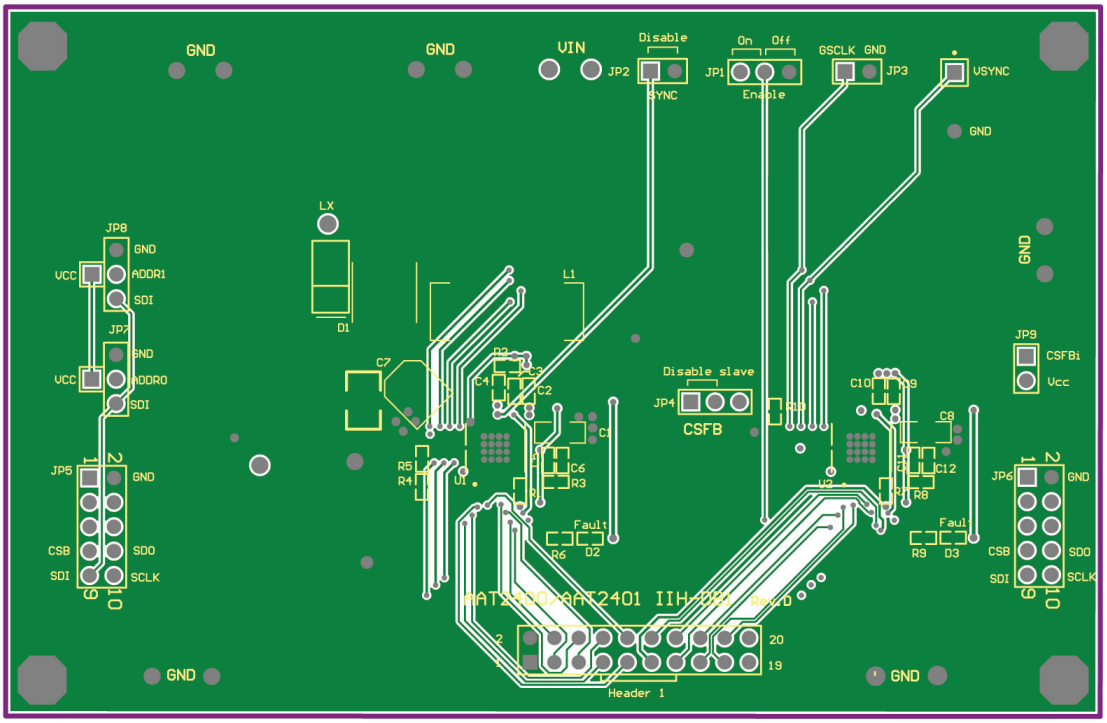


Figure 5: AAT2402M and AAT2402S Evaluation Board Middle-1 Layer Layout.

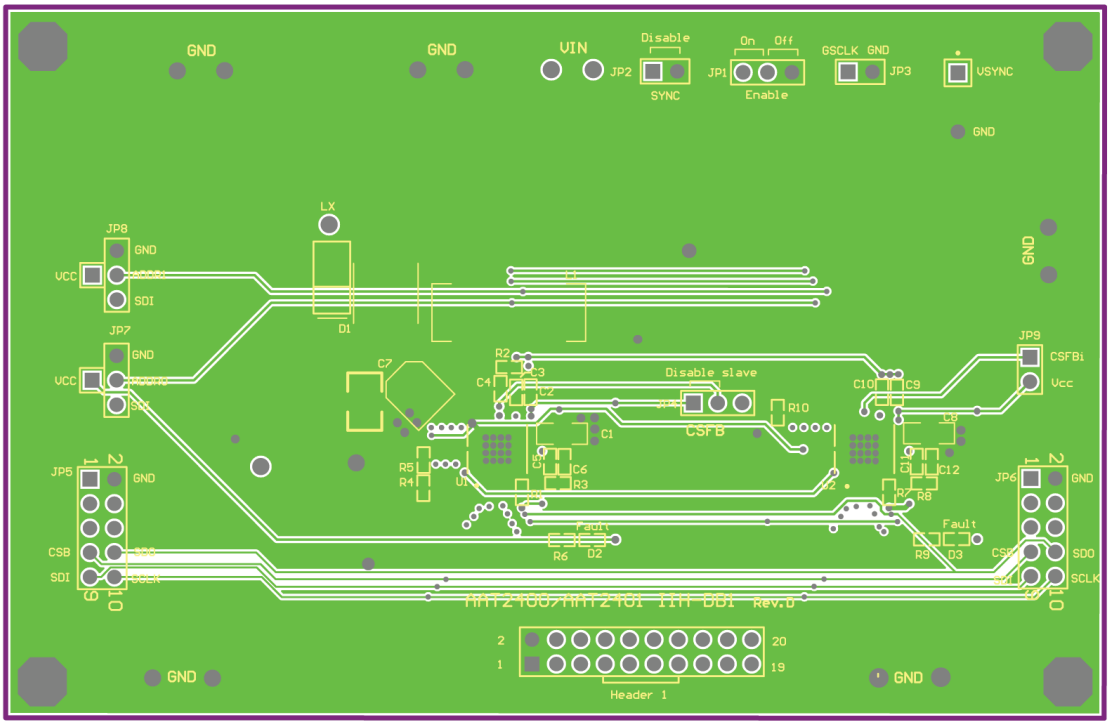


Figure 6: AAT2402M and AAT2402S Evaluation Board Middle-2 Layer Layout.

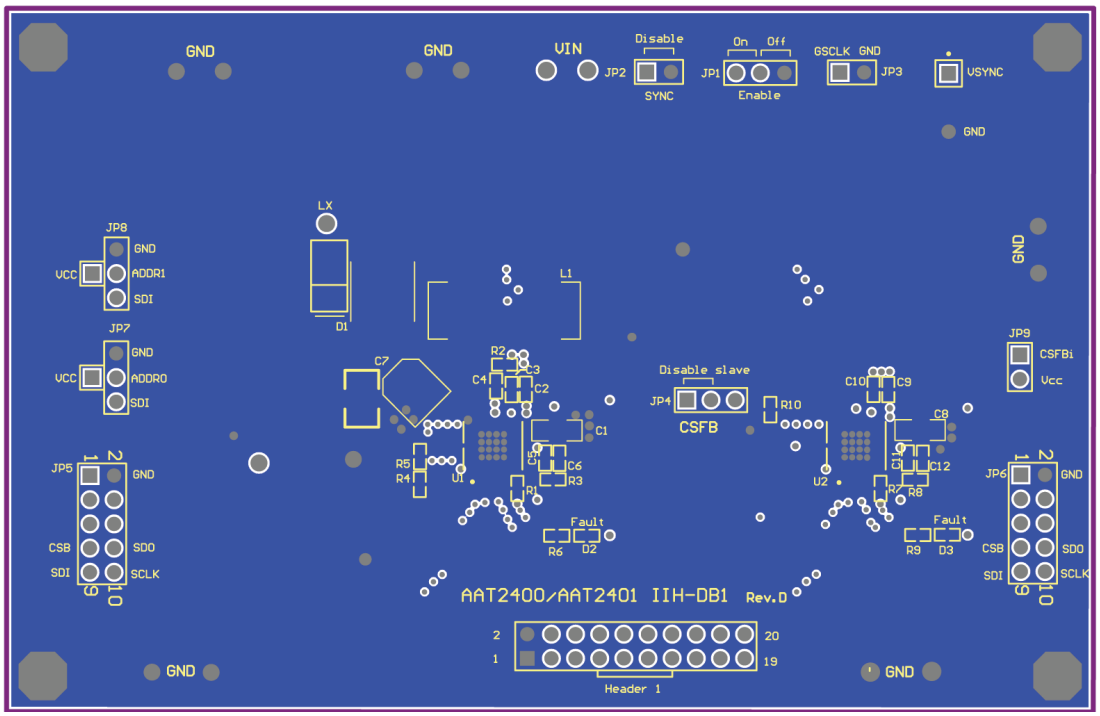


Figure 7: AAT2402M and AAT2402S Evaluation Board Bottom Side Layout.

Evaluation Board Component Lists

Component	Part Number	Description	Manufacturer
U1	AAT2402MIIH	8 Channel White LED Driver with Current and Timing Control (Master); 36 pin, 5x5 TQFN Package	Skyworks
R1	Chip Resistor	6.04kΩ, 1%, 1/4W; 0603	Vishay
R2	Chip Resistor	2kΩ, 1%, 1/4W; 0603	Vishay
R3, R5	Chip Resistor	12.1kΩ, 1%, 1/4W; 0603	Vishay
R4	Chip Resistor	442kΩ, 1%, 1/4W; 0603	Vishay
R6	Chip Resistor	2kΩ, 5%, 1/4W; 0603	Vishay
C1	GRM31CR71H475K	4.7µF, ±10%, 50V, X7R, 1206, 1.6mm	Murata
C2, C3	GRM185R60J225KE26	2.2µF, ±10%, 6.3V, X5R, 0603, 0.5mm	Murata
C4	GRM155R71H183KA12D	18nF, ±10%, 50V, X7R, 0402, 0.5mm	Murata
C5	GRM188R71A684KA61D	0.68µF, ±10%, 10V, X7R, 0603, 0.8mm	Murata
C6	GRM188R60J106M	10µF, ±10%, 6.3V, X5R, 0603, 0.8mm	Murata
C7	50CE4R7BE	4.7µF 50V Aluminum Electrolytic Capacitor	Sanyo
L1	RLF12545T-100M5R1-PF	Shield Drum Core, 10µH, 6A, 12.4mΩ	TDK
D1	MBRD360G	3.0A, 60V, SMA Schottky Barrier Rectifier	On-Semi
D2	LTST-C190CKT	Red LED; 0603	Lite-On Inc.
Header1	AWHW20G-0202-T-R	Header 10×2-Pin, Dual Row, 2.54mm	Assmann
JP1 - JP7	PRPN401PAEN	Conn. Header, 2.54mm zip	Sullins Electronics

Table 23: AAT2402M Evaluation Board Component Listing.

Component	Part Number	Description	Manufacturer
U2	AAT2402SIIH	8 Channel White LED Driver with Current and Timing Control (Slave); 36 pin, 5x5 TQFN package	Skyworks
R7	Chip Resistor	6.04kΩ, 1%, 1/4W; 0603	Vishay
R8	Chip Resistor	12kΩ, 1%, 1/4W; 0603	Vishay
R9	Chip Resistor	2kΩ, 5%, 1/4W; 0603	Vishay
R10	Chip Resistor	10kΩ, 5%, 1/4W; 0603	Vishay
C8	GRM31CR71H475K	4.7µF, ±10%, 50V, X7R, 1206, 1.6mm	MuRata
C9, C10	GRM185R60J225KE26	2.2µF, ±10%, 6.3V, X5R, 0603, 0.5mm	MuRata
C11	GRM188R71A684KA61D	0.68uF, ±10%, 10V, X7R, 0603, 0.8mm	MuRata
C12	GRM188R60J106M	10µF, ±10%, 6.3V, X5R, 0603, 0.8mm	MuRata
D3	LTST-C190CKT	Red LED; 0603	Lite-On Inc.

Table 24: AAT2402S Evaluation Board Component Listing.

Component	Part#	Description	Manufacturer
LED	SSC-ZWT715	60mA LCD Backlighting LED	Seoul Semiconductor
Cable	H3CCS--1006G-ND	Double Ended Socket Cable	Assmann

Table 25: Component Listing for LED Board.

Register Summary Table

Name	Addr	Default	D7	D6	D5	D4	D3	D2	D1	D0
DOT1	00h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT2	02h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT3	04h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT4	06h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT5	08h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT6	0Ah	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT7	0Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT8	0Eh	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT9	10h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT10	12h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT11	14h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT12	16h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT13	18h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT14	1Ah	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT15	1Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOT16	1Eh	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS1 LSB	40h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS1 MSB	42h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS2 LSB	44h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS2 MSB	46h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS3 LSB	48h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS3 MSB	4Ah	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS4 LSB	4Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS4 MSB	4Eh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS5 LSB	50h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS5 MSB	52h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS6 LSB	54h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS6 MSB	56h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS7 LSB	58h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS7 MSB	5Ah	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS8 LSB	5Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS8 MSB	5Eh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS9 LSB	60h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS9 MSB	62h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS10 LSB	64h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS10 MSB	66h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS11 LSB	68h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS11 MSB	6Ah	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS12 LSB	6Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS12 MSB	6Eh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS13 LSB	70h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS13 MSB	72h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS14 LSB	74h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS14 MSB	76h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS15 LSB	78h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS15 MSB	7Ah	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
GS16 LSB	7Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GS16 MSB	7Eh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8

Register Summary Table (continued)

Name	Addr	Default	D7	D6	D5	D4	D3	D2	D1	D0
DLY1 LSB	80h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY1 MSB	82h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY2 LSB	84h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY2 MSB	86h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY3 LSB	88h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY3 MSB	8Ah	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY4 LSB	8Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY4 MSB	8Eh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY5 LSB	90h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY5 MSB	92h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY6 LSB	94h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY6 MSB	96h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY7 LSB	98h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY7 MSB	9Ah	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY8 LSB	9Ch	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY8 MSB	9Eh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY9 LSB	A0h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY9 MSB	A2h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY10 LSB	A4h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY10 MSB	A6h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY11 LSB	A8h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY11 MSB	AAh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY12 LSB	ACh	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY12 MSB	AEh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY13 LSB	B0h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY13 MSB	B2h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY14 LSB	B4h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY14 MSB	B6h	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY15 LSB	B8h	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY15 MSB	BAh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
DLY16 LSB	BCh	00h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLY16 MSB	BEh	00h	x	x	x	x	Bit 11	Bit 10	Bit 9	Bit 8
CTL1	C0h	00h	CS8 ON	CS7 ON	CS6 ON	CS5 ON	CS4 ON	CS3 ON	CS2 ON	CS1 ON
CTL2	C2h	00h	CS16 ON	CS15 ON	CS14 ON	CS13 ON	CS12 ON	CS11 ON	CS10 ON	CS9 ON
Fault1	E0h	00h	CS4	CS4	CS3	CS3	CS2	CS2	CS1	CS1
Fault2	E2h	00h	CS8	CS8	CS7	CS7	CS6	CS6	CS5	CS5
Fault3	E4h	00h	CS12	CS12	CS11	CS11	CS10	CS10	CS9	CS9
Fault4	E6h	00h	CS16	CS16	CS15	CS15	CS14	CS14	CS13	CS13
OTMP1	E8h	00h	x	x	x	x	x	config	Bit 1	Bit 0
OTMP2	EAh	00h	x	x	x	x	x	config	Bit 1	Bit 0
Fault Reporting 1	F0h	AAh	CS4	CS4	CS3	CS3	CS2	CS2	CS1	CS1
Fault Reporting 2	F2h	AAh	CS8	CS8	CS7	CS7	CS6	CS6	CS5	CS5
Fault Reporting 3	F4h	AAh	CS12	CS12	CS11	CS11	CS10	CS10	CS9	CS9
Fault Reporting 4	F6h	AAh	CS16	CS16	CS15	CS15	CS14	CS14	CS13	CS13
Test Modes	FEh	00h	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

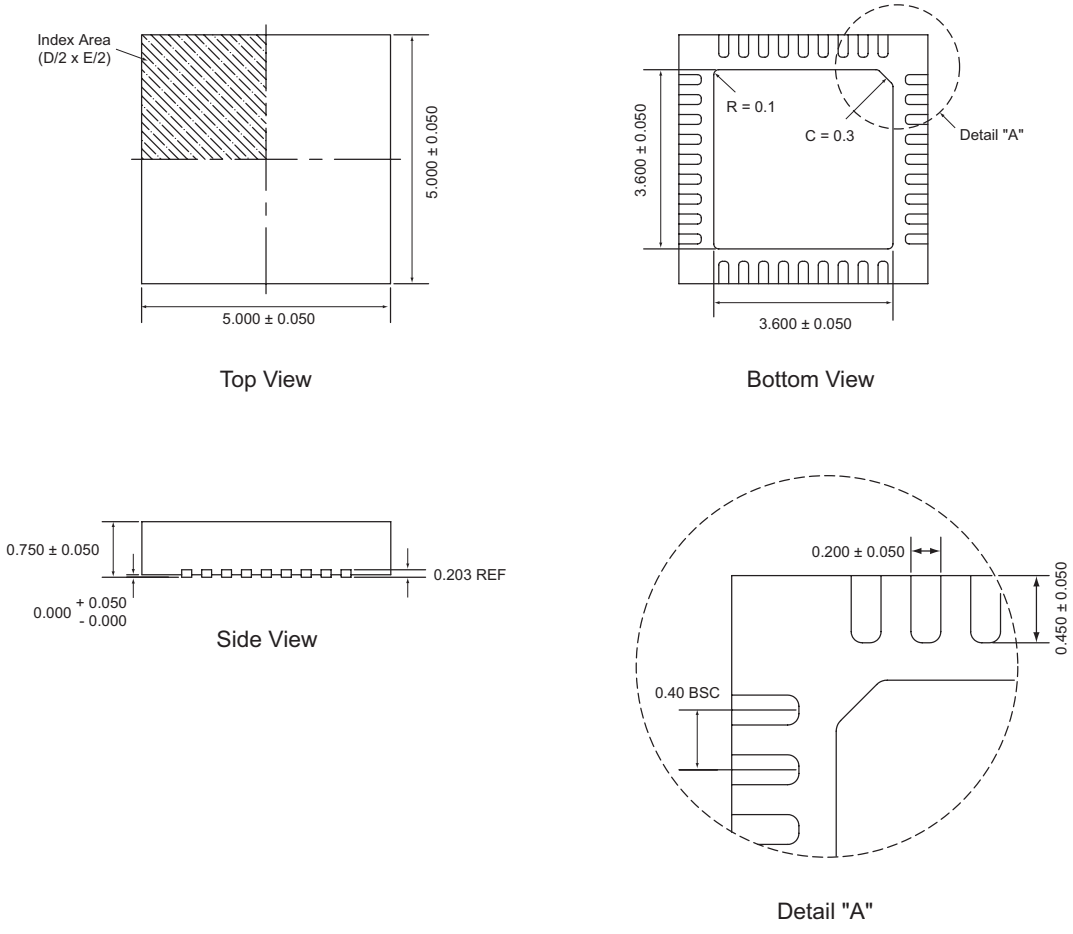
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TQFN55-36	B5XYY	**AAT2402IIH-M-T1**
TQFN55-36	B6XYY	**AAT2402IIH-S-T1**

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Package Information

TQFN55-36[3]



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN, and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.